

S/N Unknown

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kenneth W. Marr et al. Examiner: Unknown
Serial No.: Unknown Group Art Unit: Unknown
Filed: Herewith Docket: 303.819US2
Title: CIRCUITS AND METHODS TO PROTECT A GATE DIELECTRIC
ANTIFUSE

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/652429 6630724	August 31, 2000	303.674US1	GATE DIELECTRIC ANTIFUSE CIRCUITS AND METHODS FOR OPERATING SAME
10/230928	August 29, 2002	303.820US1	GATE DIELECTRIC ANTIFUSE CIRCUIT TO PROTECT A HIGH- VOLTAGE TRANSISTOR
10/680481	October 6, 2003	303.674US2	GATE DIELECTRIC ANTIFUSE CIRCUITS AND METHODS FOR OPERATING SAME

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3 Feb '04

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"Express Mail" mailing label number: EV332567705US

Date of Deposit: February 3, 2004

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to The Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria, VA 22313-1450.

CIRCUITS AND METHODS TO PROTECT A GATE DIELECTRIC ANTIFUSE

This application is a Continuation of U.S. Application No. 10/231,756, filed August 29, 2002, which is incorporated herein by reference.

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Field of the Invention

The present invention relates generally to integrated circuits, and more particularly, to circuits and methods to protect a gate dielectric antifuse.

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Background

Integrated circuits are interconnected networks of electrical components fabricated on a common foundation called a substrate. The electrical components are typically fabricated on a wafer of semiconductor material that serves as a substrate. Various fabrication techniques, such as layering, doping, masking, and etching, are used to build millions of resistors, transistors, and other electrical components on the wafer. The components are then wired together, or interconnected, to define a specific electrical circuit, such as a processor or a memory device.

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Fusible elements are employed in integrated circuits to permit changes in the configuration of the integrated circuits after fabrication. For example, fusible elements may be used to replace defective circuits with redundant circuits. Memory devices are typically fabricated with redundant memory cells. The redundant memory cells may be enabled with fusible elements after fabrication to replace defective memory cells found during a test of fabricated memory devices. Fusible elements are also used to customize the configuration of a generic integrated circuit after it is fabricated, or to identify an integrated circuit.

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One type of fusible element is a polysilicon fuse. The polysilicon fuse comprises a polysilicon conductor fabricated to conduct electrical current on an integrated circuit. A

portion of the polysilicon fuse may be evaporated or opened by a laser beam to create an open circuit between terminals of the polysilicon fuse. The laser beam may be used to open selected polysilicon fuses in an integrated circuit to change its configuration. The use of polysilicon fuses is attended by several disadvantages. Polysilicon fuses must be spaced apart from each other in an integrated circuit such that when one of them is being opened by a laser beam the other polysilicon fuses are not damaged. A bank of polysilicon fuses therefore occupies a substantial area of an integrated circuit. In addition, polysilicon fuses cannot be opened once an integrated circuit is placed in an integrated circuit package, or is encapsulated in any manner.

Another type of fusible element is an antifuse. An antifuse comprises two conductive terminals separated by an insulator or a dielectric, and is fabricated as an open circuit. The antifuse is programmed by applying a high voltage across its terminals to rupture the insulator and form an electrical path between the terminals.

Antifuses have several advantages that are not available with fuses. A bank of antifuses takes up much less area of an integrated circuit because they are programmed by a voltage difference that can be supplied on wires connected to the terminals of each of the antifuses. The antifuses may be placed close together in the bank, and adjacent antifuses are not at risk when one is being programmed. Antifuses may also be programmed after an integrated circuit is placed in an integrated circuit package, or encapsulated, by applying appropriate signals to pins of the package. This is a significant advantage for several reasons. First, an integrated circuit may be tested after it is in a package, and may then be repaired by replacing defective circuits with redundant circuits by programming selected antifuses. A generic integrated circuit may be tested and placed in a package before it is configured to meet the specifications of a customer. This reduces the delay between a customer order and shipment. The use of antifuses to customize generic integrated circuits also improves the production yield for integrated circuits because the same generic integrated circuit may be produced to meet the needs of a wide variety of customers.

Despite their advantages, the use of antifuses in integrated circuits is limited by a lack of adequate circuitry to support the programming and reading of the antifuses. There exists a need for improved circuits and methods for programming and reading antifuses in integrated circuits.

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Summary of the Invention

The above mentioned and other deficiencies are addressed in the following detailed description. According to embodiments of the present invention, an antifuse circuit is operated by coupling an elevated voltage to a first terminal of an antifuse, controlling current in the antifuse with a program driver circuit coupled to a second terminal of the antifuse, and shunting current around the antifuse with a bypass circuit coupled between the first terminal of the antifuse and the program driver circuit to protect the antifuse. The antifuse includes a layer of gate dielectric between the first terminal and the second terminal.

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15 The embodiments of the present invention protect a gate dielectric antifuse, and facilitate all the advantages associated with the use of antifuses in integrated circuits.

Brief Description of the Drawings

Figure 1 is a cross-sectional view of an antifuse according to an embodiment of the present invention.

20 Figure 2 is a block diagram of support circuits for antifuses according to an embodiment of the present invention.

Figure 3 is a cross-sectional view of a high-voltage transistor according to an embodiment of the present invention.

25 Figure 4 is a cross-sectional view of a high-voltage transistor according to an embodiment of the present invention.

Figure 5A is an electrical schematic diagram of support circuits for antifuses according to an embodiment of the present invention.

Figure 5B is an electrical schematic diagram of support circuits for antifuses according to an embodiment of the present invention.

Figure 5C is an electrical schematic diagram of support circuits for antifuses according to an embodiment of the present invention.

5 Figure 6 is a timing diagram for programming an antifuse according to an embodiment of the present invention.

Figure 7A is an electrical schematic diagram of support circuits for antifuses according to an embodiment of the present invention.

10 Figure 7B is an electrical schematic diagram of support circuits for antifuses according to an embodiment of the present invention.

Figure 7C is an electrical schematic diagram of support circuits for antifuses according to an embodiment of the present invention.

Figure 8 is an electrical schematic diagram of support circuits for antifuses according to an embodiment of the present invention.

15 Figure 9 is an electrical schematic diagram of support circuits for antifuses according to an embodiment of the present invention.

Figure 10 is an electrical schematic diagram of support circuits for antifuses according to an embodiment of the present invention.

20 Figure 11 is an electrical schematic diagram of support circuits for antifuses according to an embodiment of the present invention.

Figure 12 is an electrical schematic diagram of support circuits for antifuses according to an embodiment of the present invention.

Figure 13 is a block diagram of a static random access memory device according to an embodiment of the present invention.

25 Figure 14 is an electrical schematic diagram of an integrated circuit package according to an embodiment of the present invention.

Figure 15 is a block diagram of an information-handling system according to an embodiment of the present invention.

Detailed Description

In the following detailed description of exemplary embodiments of the present invention, reference is made to the accompanying drawings which form a part hereof, and
5 in which are shown by way of illustration specific exemplary embodiments in which the present invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical, electrical and other changes may be made without departing from the spirit or scope of
10 the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the claims.

The terms wafer and substrate may be used in the following description and include any structure having an exposed surface with which to form an integrated circuit (IC) according to embodiments of the present invention. The term substrate is understood
15 to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during fabrication, and may include other layers that have been fabricated thereupon. The term substrate includes doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor, or semiconductor layers supported by an insulator, as well as other semiconductor structures well known to
20 one skilled in the art. The term insulator is defined to include any material that is less electrically conductive than materials generally referred to as conductors by those skilled in the art.

The term “horizontal” is defined as a plane substantially parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the
25 wafer or substrate. The term “vertical” refers to a direction substantially perpendicular to the horizontal as defined above. Prepositions, such as “on,” “upper,” “side” (as in “sidewall”), “higher,” “lower,” “over,” and “under” are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate,

regardless of the orientation of the wafer or substrate. The prepositions “on,” “upper,” “side,” “higher,” “lower,” “over,” and “under” are thereby defined with respect to “horizontal” and “vertical.”

Antifuses and transistors described herein according to embodiments of the present invention may have wells that may be formed in other wells or tanks rather than substrates. Such wells or tanks may be situated with other wells or tanks, or within other wells or tanks, in a larger substrate. The wells or tanks may also be situated in a silicon-on-insulator (SOI) device.

The term “source/drain” refers generally to the terminals or diffusion regions of a field effect transistor. A terminal or a diffusion region may be more specifically described as a “source” or a “drain” on the basis of a voltage applied to it when the field effect transistor is in operation.

P-type conductivity is conductivity associated with holes in a semiconductor material, and n-type conductivity is conductivity associated with electrons in a semiconductor material. Throughout this specification the designation “n+” refers to semiconductor material that is heavily doped n-type semiconductor material, e.g., monocrystalline silicon or polycrystalline silicon. Similarly, the designation “p+” refers to semiconductor material that is heavily doped p-type semiconductor material. The designations “n-” and “p-” refer to lightly doped n and p-type semiconductor materials, respectively.

In this description a transistor is described as being activated or switched on when it is rendered conductive by a control gate voltage that is separated from its source voltage by at least its threshold voltage. The transistor is described as being in an inactive state or switched off when the control gate voltage is separated from its source voltage by less than the threshold voltage and the transistor is rendered non-conductive. A digital signal of 1 may be called a high signal and a digital signal of 0 may be called a low signal. Embodiments of the present invention described herein may be coupled to receive a power supply voltage V_{cc} which is within approximately 1 to 5 volts. By way of

example in this description, and not by way of limitation, V_{cc} is approximately 3 volts. Embodiments of the present invention described herein may be coupled to receive a ground voltage reference V_{ss} , and a bulk node voltage V_{bb} . The voltage V_{bb} may be approximately equal to V_{ss} , or may be slightly less than V_{ss} such as approximately minus 1 to minus 2 volts. V_{bb} is often coupled to p-type wells and p-type substrates in integrated circuits described herein. V_{cc} , V_{ss} , and V_{bb} are received directly or are generated by circuits that are not shown for purposes of brevity, but are known to those skilled in the art.

A cross-sectional view of an antifuse 100 according to an embodiment of the present invention is shown in Figure 1. An n-type well 110 is formed in a p-type substrate 112, and an n+-type diffusion region 114 is formed in the well 110. The n+-type diffusion region 114 provides an ohmic contact for the well 110. A p-type gate electrode 120 is formed over a layer of gate dielectric 122 which is formed over the well 110. One or more spacers 123 are formed on the sides of the gate dielectric 122 and the gate electrode 120. The gate electrode 120 is connected to a first terminal 124 of the antifuse 100, and a second terminal 126 is connected to the n+-type diffusion region 114. In alternate embodiments of the present invention the gate electrode 120 comprises polysilicon or layers of polysilicon and a silicide such as tungsten silicide (WSi_x), titanium silicide ($TiSi_2$), or cobalt silicide ($CoSi_2$). The gate dielectric 122 may be oxide, oxynitride, or nitrated oxide. A p+-type diffusion region 130 is formed in the substrate 112 to provide an ohmic contact coupling the substrate 112 to V_{bb} .

Two separate circuits in an integrated circuit may be connected respectively to the first and second terminals 124, 126 of the antifuse 100. The antifuse 100 is an open circuit between the terminals until it is programmed in the following manner. The p-type substrate 112 is coupled to V_{bb} and the first terminal 124 attached to the p-type gate electrode 120 is coupled to a positive elevated voltage, such as approximately 7-8 volts. The second terminal 126 is coupled to bring the well 110 to a low voltage. A voltage drop between the well 110 and the p-type gate electrode 120 is enough to rupture the gate

dielectric 122. When programmed the antifuse 100 has a conductive connection between the first and second terminals 124, 126 which may be biased appropriately such that the p-n junction between the p-type gate electrode 120 and the well 110 allows current to flow. The programmed antifuse 100 is an impedance element between the circuits.

5 The gate dielectric 122 may be fabricated to be thinner than gate dielectrics in conventional field effect transistors to reduce the voltage drop necessary to rupture the gate dielectric 122. The antifuse 100 with a thinner gate dielectric 122 would be programmable with a lower elevated voltage, and thus reduce the effects of the elevated voltage on neighboring circuits. The antifuse 100 may be formed in a semiconductor
10 layer formed over an insulator according to alternate embodiments of the present invention.

 The antifuse 100 described above may be used for a variety of purposes in an integrated circuit. For example, the antifuse 100 may be programmed to provide a coupling to redundant circuits, to change a configuration of the integrated circuit, to tie a
15 line to a voltage or to Vss, to change the timing of the integrated circuit, or to provide identification for the integrated circuit. The integrated circuit may be a memory device, a processor, or any other type of integrated circuit device by way of example and not by way of limitation. One or more registers of the antifuse 100 may be programmed to comprise an electrically programmable read-only memory (EPROM).

20 A large number of antifuses such as the antifuse 100 described above are arranged in banks of antifuses in an integrated circuit. A single antifuse bank 200 in an integrated circuit is shown in a block diagram in Figure 2 according to an embodiment of the present invention. An antifuse 210 has a first terminal coupled to an external pin 220 through a common bus line 230, and a second terminal coupled to a program driver circuit 242.
25 The antifuse 210 has the structure and operational method of the antifuse 100 described above, and is represented by a triangle inscribed with the letter A. The program driver circuit 242 is used to select the antifuse 210 to be programmed during a programming mode of operation. A read circuit 244 is coupled to the antifuse 210 through the program

driver circuit 242 to read a state of the antifuse 210 during an active mode of operation. A gate bias circuit 254 is coupled between the external pin 220 through the common bus line 230 and the program driver circuit 242.

The antifuse 210, the program driver circuit 242, and the read circuit 244
5 comprise a single antifuse module 260 in the antifuse bank 200. Other antifuse modules 262 and 264 each include a single antifuse coupled to a program driver circuit and a read circuit similar to those elements in the antifuse module 260. The gate bias circuit 254 is coupled between the common bus line 230 and the program driver circuits in each of the antifuse modules 260, 262, and 264 according to the embodiment of the present
10 invention. The antifuse bank 200 includes other antifuse modules similar to the antifuse module 260 which are not shown for purposes of brevity. The antifuse bank 200 may include hundreds or thousands of antifuse modules (not shown) similar to the antifuse module 260, each antifuse module being coupled to the gate bias circuit 254 which is a global circuit in the antifuse bank 200. A bypass circuit 270 is coupled in parallel with
15 the antifuse 210 between the common bus line 230 and the program driver circuit 242 in each of the antifuse modules 260, 262, and 264 according to an embodiment of the present invention. In other embodiments of the present invention a pre-charge circuit 272 is coupled between the common bus line 230 and the program driver circuit 242 in each of the antifuse modules 260, 262, and 264. All of the other antifuse modules (not shown)
20 in the antifuse bank 200 are coupled to the pre-charge circuit 272 which is a global circuit in the antifuse bank 200. The bypass circuit 270 and the pre-charge circuit 272 are used to protect the antifuse 210 in alternate embodiments of the present invention as will be described hereinbelow.

During the programming mode, an elevated voltage is applied to the external pin
25 220 and the common bus line 230 that exceeds V_{cc} of the integrated circuit by a substantial amount. The elevated voltage provides the potential necessary to rupture the gate dielectrics of antifuses selected to be programmed. The elevated voltage is removed from the external pin 220 during the active mode and during a sleep mode of operation

and the integrated circuit operates from Vcc. During the active mode and the sleep mode, the external pin 220 may be coupled to Vcc or to a different read voltage. The use of the external pin 220 to couple the elevated voltage to the antifuse 210 during the programming mode substantially protects other portions of the integrated circuit from
5 damage that may be caused by the elevated voltage.

The gate bias circuit 254 is coupled to program driver circuits for each of the other antifuse modules in the antifuse bank 200 to bias a gate of a transistor in each program driver circuit as will be described hereinbelow. The integrated circuit includes many antifuse banks similar to the antifuse bank 200 according to alternate embodiments of the
10 present invention.

The gate bias circuit 254 and the program driver circuit 242 each include at least one high-voltage transistor (HVT). One example of such a HVT is an n-well drain transistor 300, a cross-sectional view of which is shown in Figure 3 according to an embodiment of the present invention. An n-type well 310 is formed in a drain side of a p-
15 type substrate 312, and a p-type halo implant 314 is formed in a source side of the substrate 312. An n-type lightly doped drain (LDD) 316 is implanted inside the halo implant 314. A gate 320 is formed over a layer of gate dielectric 322 which is formed over the substrate 312 between the n-type well 310 and the halo implant 314. An electrode 324 is formed over the gate 320. In alternate embodiments of the present
20 invention the gate 320 may comprise polysilicon and the electrode 324 may comprise a silicide such as tungsten silicide (WSi_x), titanium silicide (TiSi_2), or cobalt silicide (CoSi_2). The gate dielectric 322 may be oxide, oxynitride, or nitrided oxide. The gate 320 and the electrode 324 may also comprise metal. One or more spacers 326 are then formed on the sides of the gate dielectric 322, the gate 320, and the electrode 324. An
25 n+-type source diffusion region 330 is implanted inside the LDD 316 and the halo implant 314. Also, an n+-type drain diffusion region 332 is implanted in the n-type well 310. The drain diffusion region 332 is not surrounded by LDD or halo implants which are blocked from the drain side of the substrate 312. A source terminal 340 is connected

to the source diffusion region 330, a gate terminal 342 is connected to the electrode 324, and a drain terminal 344 is connected to the drain diffusion region 332. A p⁺-type diffusion region 360 is formed in the substrate 312 to provide an ohmic contact coupling the substrate 312 to V_{bb}.

5 The n-well drain transistor 300 has a high drain breakdown voltage. In operation the substrate 312 is coupled to V_{bb} and the drain terminal 344 is coupled to a line with a high positive voltage, such as the common bus line 230 shown in Figure 2 during the programming mode. The n-well drain transistor 300 will break down and allow current to flow between the drain terminal 344 and the substrate 312 when a critical electric field
10 intensity (E) is reached across a boundary between the n-type well 310 and the p-type substrate 312. E may be approximated as the voltage drop across the boundary divided by a width of a depletion region at the boundary of the n-type well 310 and the p-type substrate 312. Dopant concentrations in the n-type well 310 and the p-type substrate 312 are relatively low such that the width of the depletion region between the two is relatively
15 large. The boundary will not break down even under a very large voltage drop across the boundary because the E is less than the critical E. As a result, the n-well drain transistor 300 will not break down even if the voltage on the drain terminal 344 is relatively high. In contrast, an ordinary n-channel transistor does not have the n-type well 310, and there is a boundary between a p-type substrate and an n⁺-type drain diffusion region with a
20 very high dopant concentration. A depletion region at this boundary is not very wide, and as a consequence it will break down under a smaller voltage.

A cross-sectional view of an n-channel transistor 400 is shown in Figure 4 according to an embodiment of the present invention. The transistor 400 is a HVT. A gate 420 is formed over a layer of gate dielectric 422 which is formed over a p-type
25 substrate 412. An electrode 424 is formed over the gate 420. A p-type halo implant 410 is formed in a source side of the substrate 412. An n-type lightly doped drain (LDD) 416 is implanted inside the halo implant 410. In alternate embodiments of the present invention the gate 420 comprises polysilicon and the electrode 424 may comprise a

silicide such as tungsten silicide (WSi_x), titanium silicide (TiSi_2), or cobalt silicide (CoSi_2). The gate 420 and the electrode 424 may comprise metal. The gate dielectric 422 may be oxide, oxynitride, or nitrided oxide. One or more spacers 426 are then formed on the sides of the gate dielectric 422, the gate 420, and the electrode 424. An n+-type source diffusion region 430 is implanted inside the LDD 416 and the halo implant 410. Also, an n+-type drain diffusion region 432 is implanted in the substrate 412. The drain diffusion region 432 is not surrounded by LDD or halo implants which are blocked from a drain side of the substrate 412. A source terminal 440 is connected to the source diffusion region 430, a gate terminal 442 is connected to the electrode 424, and a drain terminal 444 is connected to the drain diffusion region 432. The drain diffusion region 432 and the source diffusion region 430 are self-aligned with the spacers 426. A p+-type diffusion region 460 is formed in the substrate 412 to provide an ohmic contact coupling the substrate 412 to V_{bb} . In another embodiment of the present invention, an added mask and implant could be applied to the drain diffusion region 432 to customize the high drain breakdown voltage of the n-channel transistor 400. The n-channel transistor 400 has a high drain breakdown voltage and may be used in embodiments of the present invention described above in place of the n-well drain transistor 300 shown in Figure 3.

The transistors 300 and 400 shown in Figures 3 and 4 may be fabricated according to process steps used to fabricate field-effect transistors in an integrated circuit, and do not require extra process steps.

Several of the circuits in the antifuse bank 200 shown in Figure 2 are shown in greater detail in Figure 5A. An electrical schematic diagram of several support circuits 500 for programming and reading antifuses is shown in Figure 5A according to an embodiment of the present invention. The circuits 500 include a gate bias circuit 508, a pre-charge circuit 509, a program driver circuit 510, and a read circuit 511. A gate electrode 514 of an antifuse 516 is coupled through a common bus line 520 to an external pin 522, and the program driver circuit 510 is coupled to a well 523 of the antifuse 516. The antifuse 516 is similar in structure and operation to the antifuse 100 shown in Figure

1. The gate bias circuit 508 is coupled to other program driver circuits (not shown) in the antifuse bank 200.

The gate electrode 514 or the well 523 of the antifuse 516 may be coupled to the common bus line 520, with the other end of the antifuse 516 being coupled to the
5 program driver circuit 510 according to alternate embodiments of the present invention. The antifuse 516 may be coupled to the common bus line 520 such that, if it has a p/n junction of p-type material and n-type material after being programmed, the p/n junction will be forward biased during the active mode of operation to present a low impedance to current flow.

10 The program driver circuit 510 includes a HVT 524 having a drain terminal 526, a source terminal 528, and a gate terminal 530. The HVT 524 is similar in structure and operating characteristics to the n-channel transistor 400 shown in Figure 4. The drain terminal 526 is coupled to the well 523 of the antifuse 516. The gate terminal 530 is coupled to the gate bias circuit 508, and the gate bias circuit 508 is coupled to the
15 common bus line 520 and the external pin 522. Current will flow through the HVT 524 as long as the other elements of the circuits 500 allow current to flow, as will be described hereinbelow. The gate bias circuit 508 couples the gate terminal 530 to a selected voltage as will be described hereinbelow. The pre-charge circuit 509 is coupled between the common bus line 520 and the source terminal 528 of the HVT 524 to provide
20 current to protect the antifuse 516 as will be described hereinbelow.

The program driver circuit 510 also includes a first n-channel transistor 540 and a second n-channel transistor 541 coupled in cascode between the source terminal 528 and Vss. A gate terminal of the transistor 540 is coupled to Vcc, and the transistor 540 is switched on as long as Vcc exceeds a voltage at its source terminal by a threshold voltage
25 V_T of the transistor 540. A gate terminal of the transistor 541 is coupled to a select logic circuit SEL 542 that controls the program driver circuit 510 during the programming, active, and sleep modes. A body terminal of the transistor 541 is coupled to Vbb. The transistor 541 is switched off by the logic circuit SEL 542 in each of the programming,

active, and sleep modes, and is switched on for a short period to program the antifuse 516 during the programming mode.

5 An n-channel transistor 543 is coupled in parallel with the transistor 541 between the transistor 540 and Vss. A gate terminal of the transistor 543 is coupled to a control logic circuit CTLG 544 that controls current through the transistor 543. The transistor 543 is a long-L transistor that may conduct between approximately 0.06 and 1 microamps, and is switched on by the control logic circuit CTLG 544 during the active mode as will be described hereinbelow.

10 An n-channel transistor 545 is coupled in parallel with the transistors 541 and 543 between the transistor 540 and Vss. A gate terminal of the transistor 545 is coupled to a control logic circuit CTLT 546 that controls current through the transistor 545. The transistor 545 is a short-L transistor that may conduct between approximately 1-28 microamps, and is switched on by the control logic circuit CTLT 546 during the active mode as will be described hereinbelow.

15 The common bus line 520 is coupled to receive an elevated voltage during the programming mode, for example approximately 7-8 volts, through the external pin 522. Before the antifuse 516 is programmed the elevated voltage on the common bus line 520 is distributed across the antifuse 516, and the transistors 524, 540, 541, 543, and 545 which are non-linear elements. Each of the antifuse 516 and the transistors 524, 540, 20 541, 543, and 545 in the program driver circuit 510 bears a portion of the elevated voltage in a manner similar to a capacitor divider circuit. The distribution of the elevated voltage is non-linear and may vary over time. When the antifuse 516 is programmed, it is an impedance element and the distribution of the elevated voltage changes. Voltages along the program driver circuit 510 rise as the antifuse 516 is programmed, and the elevated 25 voltage is distributed across the antifuse 516 and the transistors 524, 540, 541, 543, and 545 in a manner similar to a resistor divider circuit. Each of the antifuse 516 and the transistors 524, 540, 541, 543, and 545 bears a portion of the elevated voltage.

The antifuse 516 may be selected to be programmed by the logic circuit SEL 542 by switching on the transistor 541 to conduct current from the common bus line 520 through to Vss. The transistor 541 is switched on for a short period of time to allow the elevated voltage on the common bus line 520 to rupture a gate dielectric in the antifuse 516, and is then switched off. A timing diagram 600 of a voltage V_{526} at the drain terminal 526 of the HVT 524 during the programming of the antifuse 516 is shown in Figure 6 according to an embodiment of the present invention. The voltage V_{526} is shown on a vertical axis and time is shown on a horizontal axis. Starting at a time t_0 the voltage V_{526} is high at V_1 and the program driver circuit 510 behaves as a capacitor divider circuit during a period 602 until a time t_1 when the transistor 541 is switched on. The voltage V_{526} then falls quickly to a low voltage V_2 that is near Vss. The antifuse 516 undergoes a percolation period 604 between times t_2 and t_3 while the antifuse 516 remains intact under a significant voltage drop between the elevated voltage and V_2 . The percolation period may last approximately from 1/2 to 1 microsecond. The gate dielectric in the antifuse 516 ruptures between times t_3 and t_4 and the voltage V_{526} rises to V_3 after time t_4 . The antifuse 516 is an impedance element after time t_4 and the program driver circuit 510 bears the elevated voltage in a manner similar to a resistor divider circuit. The transistor 541 remains switched on after time t_4 during a soak period 606 of approximately 10 milliseconds to permit a delivered energy to thoroughly rupture the gate dielectric in the antifuse 516. The energy delivered to the gate dielectric is approximately equal to the current through the antifuse 516 during the soak period 606 multiplied by the voltage drop across the antifuse 516 and divided by the time of the soak period 606. The voltage V_{526} remains at V_3 during the soak period 606 while the transistor 541 is switched on.

The read circuit 511 includes elements used to read a state of the antifuse 516, and these elements will now be described according to an embodiment of the present invention. The read circuit 511 also includes the transistor 543, the control logic circuit CTLG 544, the transistor 545, and the control logic circuit CTLT 546. The program driver circuit 510 is also coupled to the read circuit 511 through an n-channel pass-gate

transistor 550. A drain of the pass-gate transistor 550 is coupled to the source terminal 528 of the HVT 524, and a source of the pass-gate transistor 550 is coupled to a gate of an n-channel transistor 552. A sleep signal ZZ* is coupled to a gate of the pass-gate transistor 550 and to a gate of a p-channel transistor 554. The sleep signal ZZ* is an
5 active-low signal that is high during the active mode to switch on the pass-gate transistor 550 and low during the sleep mode to switch off the pass-gate transistor 550. The transistor 554 has a source coupled to Vcc and a drain coupled to the source of the pass-gate transistor 550 and the gate of the transistor 552. The transistor 552 has a source coupled to Vss and a drain coupled to a drain of a p-channel transistor 556. A source of
10 the transistor 556 is coupled to Vcc. A gate of the transistor 556 is coupled to a bias signal BIAS, which configures the transistor 556 as a bandgap-based current source. The drains of the transistors 552 and 556 generate an output signal OUTPUT at an output indicating the state of the antifuse 516 during the active mode.

During the active and sleep modes of operation, the common bus line 520 and the
15 external pin 522 are coupled to a read voltage VREAD according to an embodiment of the present invention. The read voltage VREAD may be more or less or approximately equal to Vcc. The read voltage VREAD is supplied from a source external to the circuits 500 through the external pin 522, and this is called supply stealing.

The elevated voltage and the read voltage VREAD are coupled to the common
20 bus line 230 or the common bus line 520 from a driver circuit instead of the external pins 220 or 522 according to alternate embodiments of the present invention. The driver circuit is located in the antifuse bank 200 or the circuits 500. The entire disclosure of U.S. Application Serial No. 09/652,429 entitled GATE DIELECTRIC ANTIFUSE CIRCUITS AND METHODS FOR OPERATING SAME and filed on August 31, 2000, is
25 incorporated herein by reference. The application Serial No. 09/652,429 discloses a driver circuit and other circuits that are used with and coupled to the circuits described herein according to alternate embodiments of the present invention.

The read circuit 511 generates the output signal OUTPUT in the following manner. The pass-gate transistor 550 is switched off and the transistor 554 is switched on during the sleep mode by the sleep signal ZZ*. The gate of the transistor 552 is coupled through the transistor 554 to Vcc to switch on the transistor 552 to generate a low

5 OUTPUT signal at the drain of the transistor 552.

The pass-gate transistor 550 is switched on and the transistor 554 is switched off during the active mode by the sleep signal ZZ*. One of the transistors 543 and 545 is also switched on during the active mode by the control logic circuit CTLG 544 or CTLT 546 to draw current through the transistor 540, which is always switched on, to Vss. The
10 HVT 524 is switched on by the gate bias circuit 508 during the active mode.

The state of the antifuse 516 is read in the following manner. If the antifuse 516 is programmed and has a low impedance, a voltage that is approximately VREAD less a threshold voltage V_T of the HVT 524 will be coupled to the gate of the transistor 552 to switch it on to couple the drain of the transistor 552 to Vss and generate a low OUTPUT
15 signal. If the antifuse 516 is unprogrammed it will have a high impedance and its dielectric will substantially insulate the read circuit 511 from VREAD on the common bus line 520. The transistor 543 or 545 that is switched on during the active mode will draw current from the read circuit 511 through the transistor 540 to Vss to leave a low voltage coupled to the gate of the transistor 552. The transistor 552 is switched off, and
20 the drains of the transistors 552 and 556 are coupled to Vcc through the transistor 556 to generate a high OUTPUT signal to indicate that the antifuse 516 is unprogrammed.

When unprogrammed, the antifuse 516 can be damaged by undesirable currents. For example, the antifuse 516 and the transistors 524, 540, 541, 543, and 545 behave as a capacitor divider circuit with respect to voltages on the common bus line 520 when the
25 antifuse 516 is unprogrammed. The antifuse 516 behaves as a first capacitor with a relatively small capacitance, and the transistors 524, 540, 541, 543, and 545 behave collectively as a second capacitor with a relatively large capacitance. The smaller relative capacitance of the unprogrammed antifuse 516 means it bears a larger portion of the

voltage on the common bus line 520 than do the transistors in the capacitor divider circuit. The antifuse 516 can bear a particularly large voltage difference during the programming mode when the elevated voltage is on the common bus line 520, and this voltage difference can result in tunneling current through the antifuse 516. The tunneling
5 current may not program the antifuse 516, but it can damage the antifuse 516 in a similar way without fully programming it.

The transistors 524, 540, 541, 543, and 545 can also have subthreshold and/or junction leakage current that will pass through the antifuse 516. If the antifuse 516 is unprogrammed, any current leakage through it will degrade its gate dielectric. It is
10 therefore advantageous to reduce sources of current leakage as much as possible.

One or more of the transistors 524, 540, 541, 543, and 545 can have reverse bias junction leakage, also called gate induced drain leakage (GIDL). The transistors 524, 540, 541, 543, and 545 are n-channel transistors each having n⁺-type source and drain regions separated by a channel region in a p-type substrate. A thin layer of oxide
15 separates the channel region from a gate electrode in each transistor. The n⁺-type drain region and the p-type substrate comprise a parasitic diode which is reverse biased by a positive voltage on the drain terminal of the transistor which occurs when the elevated voltage is on the common bus line 520. GIDL current may leak across the reverse biased parasitic diode, and this leakage can increase with an increase of an electric field intensity
20 (E) near the drain region which is increased due to the proximity of the gate electrode. GIDL current increases with a rising voltage on the drain terminal of the transistor which raises E near the drain region. GIDL current may be more of a problem in the transistors 524 and 540.

One or more of the transistors 524, 540, 541, 543, and 545 can also have
25 subthreshold current due to drain induced barrier lowering (DIBL). Each of the n-channel transistors 524, 540, 541, 543, and 545 may be switched on to conduct current between its drain and source terminals when the voltage at its gate terminal exceeds the voltage at its source terminal by a threshold voltage V_T of the transistor. The difference between the

voltage at the gate terminal and the voltage at the source terminal is called V_{GS} . DIBL leakage current flows between the drain terminal and the source terminal at a subthreshold V_{GS} , when V_{GS} is less than V_T of the transistor. DIBL leakage current therefore occurs when the transistor is switched off, and this current can damage the antifuse 516 when it is unprogrammed. The subthreshold current is increased as the voltage at the drain terminal of the transistor increases when the elevated voltage is on the common bus line 520, and the DIBL leakage current can therefore occur at lower and lower values of V_{GS} . If the voltage at the drain terminal is high enough, DIBL leakage current can occur when V_{GS} is zero. DIBL leakage current may be more of a problem in the transistors 541, 543, and 545.

The entire disclosure of U.S. Application Serial No. 09/652,429 entitled GATE DIELECTRIC ANTIFUSE CIRCUITS AND METHODS FOR OPERATING SAME and filed on August 31, 2000, is incorporated herein by reference. Application Serial No. 09/652,429 addresses the reduction of snap-back and DIBL and GIDL leakage current described above.

Free electrons in a substrate of the integrated circuit including the program driver circuit 510 can also cause unwanted current in the unprogrammed antifuse 516. The free electrons will collect in the n+-type drain diffusion region of the HVT 524 and pass through the unprogrammed antifuse 516.

Embodiments of the present invention include circuits to shunt or bypass current around the unprogrammed antifuse 516 during the programming mode to protect the antifuse 516. The circuits may be called shunt circuits or bypass circuits or pre-charge circuits and are coupled in parallel with the antifuse 516 between the common bus line 520 and the program driver circuit 510. The shunt circuits or bypass circuits or pre-charge circuits conduct current between the common bus line 520 and the program driver circuit 510 that does not pass through the antifuse 516. Examples of a shunt circuit or a bypass circuit or a pre-charge circuit include the bypass circuit 270 or the pre-charge circuit 272 shown in Figure 2 that shunt or bypass current around the antifuse 210.

Several of the circuits in the antifuse bank 200 shown in Figure 2 are shown in greater detail in Figure 5B. An electrical schematic diagram of several support circuits 560 for programming and reading antifuses is shown in Figure 5B according to an embodiment of the present invention. The circuits 560 have many elements that are similar to the elements of the circuits 500 shown in Figure 5A. Elements common to both of the circuits 500 and 560 have been given the same reference numerals and will not be described, and the details of the read circuit 511 have not been shown, for purposes of brevity.

The gate bias circuit 508 shown in Figure 5A is shown in more detail in Figure 5B. The gate bias circuit 508 includes a first impedance 562 coupled between the common bus line 520 and the gate terminal 530 of the HVT 524. The gate bias circuit 508 also includes a second impedance 564 coupled between the gate terminal 530 and a first reference voltage Vref1. The first impedance 562 and the second impedance 564 form a voltage divider and couple a voltage between Vref1 and VREAD to the gate terminal 530 during the active mode and sleep mode. Vref1 could be Vcc or Vss or any voltage between them. VREAD is on the common bus line 520 during the active mode and the sleep mode and may be more or less or approximately equal to Vcc. The first impedance 562 and the second impedance 564 couple a voltage between Vref1 and the elevated voltage to the gate terminal 530 during the programming mode of operation when the elevated voltage is on the common bus line 520. The voltage on the gate terminal 530 during the programming mode is determined by a ratio of the impedances 562 and 564, and this ratio is selected to protect the HVT 524 as will be described hereinbelow. The first impedance 562 and the second impedance 564 may each be a resistor or a transistor or other electric or electronic element that provides an electrical impedance. The first impedance 562 and the second impedance 564 may comprise a combination of different types of impedances such as a combination of a resistor and a transistor or multiple resistors and transistors or various combinations of resistors, transistors, and other elements that provide an electrical impedance.

The pre-charge circuit 509 shown in Figure 5A is shown in more detail in Figure 5B. The pre-charge circuit 509 is an analog voltage generator circuit having an impedance, and includes a third impedance 565 coupled between the common bus line 520 and an anode 566 of a diode 567. The pre-charge circuit 509 also includes a fourth impedance 568 coupled between the anode 566 of the diode 567 and a second reference voltage Vref2. Vref2 could be Vcc or Vss or any voltage between them. A cathode 569 of the diode 567 is coupled to the source terminal 528 of the HVT 524. The third impedance 565 and the fourth impedance 568 form a voltage divider and couple an analog voltage between Vref2 and the elevated voltage, less a voltage drop due to the diode 567, to the source terminal 528 of the HVT 524 during the programming mode of operation when the elevated voltage is on the common bus line 520. The program driver circuit 510 receives current from the pre-charge circuit 509 through the diode 567 to replace current lost through subthreshold current or junction leakage, or to displace free electrons in the program driver circuit 510. The pre-charge circuit 509 pre-charges the capacitive structures in the program driver circuit 510 and the read circuit 511 below the antifuse 516 before it is programmed during the programming mode. An unprogrammed antifuse 516 is protected by the current provided by the pre-charge circuit 509 that displaces current that may otherwise have been drawn through the antifuse 516. The diode 567 substantially prevents charge from migrating to the pre-charge circuit 509 during the programming mode when the antifuse 516 is programmed and there is a high voltage on the source terminal 528 of the HVT 524. The pre-charge circuit 509 is coupled to multiple antifuse modules in the antifuse bank 200 shown in Figure 2 that might otherwise be damaged by the high voltage. The third impedance 565 and the fourth impedance 568 may each be a resistor or a transistor or other electric or electronic element that provides an electrical impedance. The third impedance 565 and the fourth impedance 568 may comprise a combination of different types of impedances such as a combination of a resistor and a transistor or multiple resistors and transistors or various

combinations of resistors, transistors, and other elements that provide an electrical impedance.

Resistance values of the third impedance 565 and the fourth impedance 568 are large so that the diode 567 sources a low level of current from the common bus line 520 to the program driver circuit 510 during the programming mode.

Several of the circuits in the antifuse bank 200 shown in Figure 2 are shown in greater detail in Figure 5C. An electrical schematic diagram of several support circuits 570 for programming and reading antifuses is shown in Figure 5C according to an embodiment of the present invention. The circuits 570 have many elements that are similar to the elements of the circuits 560 shown in Figure 5B, and elements common to both of the circuits 560 and 570 have been given the same reference numerals and will not be described for purposes of brevity. The circuits 570 of Figure 5C include a gate bias circuit 571 and a pre-charge circuit 580 according to other embodiments of the present invention that replace the gate bias circuit 508 and the pre-charge circuit 509 shown in Figures 5A and 5B.

The gate bias circuit 571 includes a first adjustable resistor 572 and a HVT 574 coupled in series between the common bus line 520 and the gate terminal 530 of the HVT 524. A gate and a drain of the HVT 574 are coupled together to the first adjustable resistor 572 and a source of the HVT 574 is coupled to the gate terminal 530 such that the HVT 574 is diode-connected. The gate bias circuit 571 also includes a second adjustable resistor 576 coupled between the gate terminal 530 and Vcc. The first adjustable resistor 572, the HVT 574, and the second adjustable resistor 576 form a voltage divider. The first adjustable resistor 572, the HVT 574, and the second adjustable resistor 576 couple a voltage of between Vcc and VREAD to the gate terminal 530 during the active mode and the sleep mode when VREAD is on the common bus line 520. The first adjustable resistor 572, the HVT 574, and the second adjustable resistor 576 couple a voltage between Vcc and the elevated voltage to the gate terminal 530 during the programming mode of operation when the elevated voltage is on the common bus line 520. The voltage

on the gate terminal 530 during the programming mode is determined by a ratio of the impedances of the first adjustable resistor 572, the HVT 574, and the second adjustable resistor 576, and this ratio is selected to protect the HVT 524 as will be described hereinbelow. The first adjustable resistor 572 and the second adjustable resistor 576 may

5 comprise a combination of different types of impedances such as a combination of a resistor and a transistor or multiple resistors and transistors or various combinations of resistors, transistors, and other elements that provide an electrical impedance.

The pre-charge circuit 580 is an analog voltage generator circuit having an impedance. The pre-charge circuit 580 includes a first adjustable resistor 582, a HVT

10 584, and a second adjustable resistor 586 coupled in series between the common bus line 520 and Vcc. A gate and a drain of the HVT 584 are coupled together to the first adjustable resistor 582 such that the HVT 584 is diode-connected. A source of the HVT 584 is coupled to the second adjustable resistor 586 and to a drain of a HVT 588. A gate of the HVT 588 is coupled to Vcc, and a source of the HVT 588 is coupled to a drain of

15 an n-channel transistor 589. A source of the transistor 589 is coupled to Vss, and a gate of the transistor 589 is coupled to receive a READ/PROGRAM* signal that is more fully described hereinbelow.

A pair of top and bottom diode-connected HVTs 590 and 592 are coupled in series between the drain of the HVT 584 and the source terminal 528 of the HVT 524.

20 Each of the top and bottom diode-connected HVTs 590 and 592 have a gate and a drain coupled together, and the drain of the bottom diode-connected HVT 592 is coupled to a source of the top diode-connected HVT 590. A source of the bottom diode-connected HVT 592 is coupled to the source terminal 528 of the HVT 524. Gates and drains of the top diode-connected HVT 590 and the HVT 584 are coupled together.

25 The first adjustable resistor 582, the HVT 584, and the second adjustable resistor 586 thereby form a voltage divider to couple an analog voltage between Vcc and the elevated voltage, less a voltage drop due to the top and bottom diode-connected HVTs 590 and 592, to the source terminal 528 of the HVT 524 during the programming mode

of operation when the elevated voltage is on the common bus line 520. The analog voltage may be one threshold voltage above the voltage applied to the gate terminal 530 by the gate bias circuit 571 during the programming mode by appropriate selection of the impedances of the first adjustable resistor 582, the HVT 584, and the second adjustable resistor 586. The program driver circuit 510 receives current from the pre-charge circuit 580 through the top and bottom diode-connected HVTs 590 and 592 to replace current lost through subthreshold current or junction leakage, or to displace free electrons in the program driver circuit 510. An unprogrammed antifuse 516 is protected by the current provided by the pre-charge circuit 580 that displaces current that may otherwise have been drawn through the antifuse 516.

The top and bottom diode-connected HVTs 590 and 592 substantially prevent charge from migrating to the pre-charge circuit 580 during the programming mode when the antifuse 516 is programmed and there is a high voltage on the source terminal 528 of the HVT 524. The pre-charge circuit 580 is coupled to multiple antifuse modules in the antifuse bank 200 shown in Figure 2 that might otherwise be damaged by the high voltage.

The READ/PROGRAM* signal coupled to the gate of the transistor 589 is low during the programming mode such that the transistor 589 is switched off and a voltage at the source of the HVT 584 can rise above Vss. During the active mode, the READ/PROGRAM* signal is high to switch on the transistor 589 and couple the source of the HVT 584 to Vss through the transistor 589 and the HVT 588. The HVT 588 is switched on when the transistor 589 is switched on. Current from the common bus line 520 passes through the HVT 584, the HVT 588, and the transistor 589 to Vss during the active mode, and is thereby substantially prevented from migrating to the read circuit 511 through the top and bottom diode-connected HVTs 590 and 592 during the active mode.

The first adjustable resistor 582 and the second adjustable resistor 586 may comprise a combination of different types of impedances such as a combination of a

resistor and a transistor or multiple resistors and transistors or various combinations of resistors, transistors, and other elements that provide an electrical impedance.

Resistance values of the first adjustable resistor 582 and the second adjustable resistor 586 are large so that the top and bottom diode-connected HVTs 590 and 592
5 source a low level of current from the common bus line 520 to the program driver circuit 510 during the programming mode.

A voltage ramp rate on the common bus line 520 is not to exceed time constants of elements in the pre-charge circuit 580.

A voltage sweep of the antifuse 516 may be carried out in the following manner
10 once the antifuse 516 has been programmed to determine its resistive characteristics. The transistors 543 and 545 are switched off, and the transistor 541 is switched on by the control logic circuit CTLT 546 to control current flow through the program driver circuit 510 to Vss. A voltage on the common bus line 520 is varied and current on the common bus line 520 that passes through the program driver circuit 510 is measured to determine
15 the current/voltage characteristics of the programmed antifuse 516. The voltage on the common bus line 520 is varied above or below Vss such that data for the voltage sweep is obtained for voltages near Vss. The gate terminal 530 of the HVT 524 is maintained at approximately Vcc by the gate bias circuit 571 so that the resistance of the HVT 524 remains relatively unchanged during the sweep, and the diode-connected HVT 574
20 substantially prevents current flow from the gate bias circuit 571 to the common bus line 520 during the voltage sweep.

With reference to the antifuse bank 200 shown in Figure 2, once an antifuse such as the antifuse 210 is programmed, it is an impedance element similar to a resistor, and provides a possible current path from the common bus line 230. It is desirable to limit
25 current on the common bus line 230, and therefore additional sources of current on the common bus line 230 are to be substantially eliminated as far as is possible.

Each of the gate bias circuits 508 and 571 shown in Figures 5A, 5B, and 5C help to substantially reduce current flow through the HVT 524 from the common bus line 520

during the programming mode when the common bus line 520 is at the elevated voltage and the antifuse 516 is programmed. The elevated voltage may induce breakdown current in the HVT 524, and this does not occur through its substrate because of the high drain breakdown voltage of the HVT 524.

5 Each of the gate bias circuits 508 and 571 may substantially prevent breakdown current across the gate dielectric of the HVT 524 during the programming mode. An example is illustrated with reference to the transistor 400 and the circuits 560 shown in Figures 4 and 5B. The drain terminal 526 is connected to the drain diffusion region 432, the gate terminal 530 is connected to the electrode 424, and the source terminal 528 is
10 connected to the source diffusion region 430. The voltage at the electrode 424 is insulated from the voltage at the drain diffusion region 432 by the gate dielectric 422. However, current will flow across the gate dielectric 422 if a voltage differential between the drain diffusion region 432 and the electrode 424 is large. The gate dielectric 422 may even break down and become a resistive element if the voltage differential is large
15 enough.

 The gate bias circuit 508 in the circuits 500 and 560 raises the gate terminal 530 to a voltage between V_{ref1} and the elevated voltage during the programming mode, such that a voltage difference across the gate dielectric 422 is too small to induce current flow through the gate dielectric 422 to the electrode 424. The gate bias circuit 508 thereby
20 reduces damage to the gate dielectric 422 by reducing the voltage drop across the gate dielectric 422 when the antifuse 516 is programmed and the common bus line 520 is at the elevated voltage. If the gate terminal 530 were held at a lower voltage such as V_{ref1} , then the large voltage differential might cause continuous current and damage the gate dielectric 422 when the drain terminal 526 was near the elevated voltage. Similarly, the
25 gate bias circuit 571 in the circuits 570 raises the gate terminal 530 to a voltage between V_{cc} and the elevated voltage during the programming mode.

 The voltage on the gate terminal 530 during the programming mode is determined by the ratio of the impedances 562 and 564 in the gate bias circuit 508, or by the ratio of

the impedances of the first adjustable resistor 572, the HVT 574, and the second adjustable resistor 576 in the gate bias circuit 571. The ratios of these impedances are selected such that the voltage on the gate terminal 530 during the programming mode is high enough such that a voltage difference across the gate dielectric 422 in the HVT 524 is too small to induce current flow through the gate dielectric 422 after the antifuse 516 has been programmed, but not so high as to damage the gate dielectric 422 when the antifuse 516 is being programmed. With reference to Figure 6 and its description above, a voltage at the source terminal 528 of the HVT 524 is nearly V_{ss} during the percolation period 604 when the antifuse 516 is intact. If the voltage on the gate terminal 530 during the programming mode is too high, current may flow between the source diffusion region 430 and the electrode 424 across the gate dielectric 422, and the gate dielectric 422 may break down. The ratio of the impedances 562 and 564 in the gate bias circuit 508, or the ratio of the impedances of the first adjustable resistor 572, the HVT 574, and the second adjustable resistor 576 in the gate bias circuit 571, are selected such that the voltage on the gate terminal 530 during the programming mode is low enough to substantially prevent current flow across the gate dielectric 422 when the antifuse 516 is being programmed, and is high enough to substantially prevent current flow across the gate dielectric 422 after the antifuse 516 has been programmed.

Several of the circuits in the antifuse bank 200 shown in Figure 2 are shown in greater detail in Figure 7A. An electrical schematic diagram of several support circuits 700 for programming and reading antifuses is shown in Figure 7A according to an embodiment of the present invention. The circuits 700 have many elements that are similar to the elements of the circuits 500 shown in Figure 5A, and elements common to both of the circuits 500 and 700 have been given the same reference numerals and will not be described for purposes of brevity. The circuits 700 of Figure 7A include a bypass circuit 702 according to an embodiment of the present invention. The bypass circuit 702 shunts or bypasses current around the antifuse 516 in a manner similar to the bypass circuit 270 of the antifuse bank 200 shown in Figure 2.

The bypass circuit 702 includes multiple diodes 704 coupled in series between the common bus line 520 and the well 523 of the antifuse 516. Three diodes 704 are shown in the bypass circuit 702, but more or less than three diodes 704 may be included in the bypass circuit 702 according to alternate embodiments of the present invention. An
5 anode of one of the diodes 704 is coupled to the common bus line 520, and a cathode of another one of the diodes 704 is coupled to the well 523 of the antifuse 516. Others of the diodes 704 have an anode coupled to a cathode of a preceding diode 704, and a cathode coupled to an anode of a succeeding diode 704. The diodes 704 shunt or bypass a low level of current around the antifuse 516 from the common bus line 520 to the
10 program driver circuit 510 during the programming mode when the elevated voltage is on the common bus line 520. The antifuse 516 is programmed when the transistor 541 is switched on, and the transistor 541 draws substantially more current than the diodes 704 can pass such that a sufficient voltage difference is applied to program the antifuse 516.

The number of diodes 704 coupled together in the bypass circuit 702 is selected
15 such that current drawn through the bypass circuit 702 is less than ten percent of a load current that would be drawn through the antifuse 516 if it were being read after having been programmed. The number of diodes 704 is selected assuming the worst-case operating conditions of the circuits 700 including such conditions as operating temperature and Vcc.

20 Several of the circuits in the antifuse bank 200 shown in Figure 2 are shown in greater detail in Figure 7B. An electrical schematic diagram of several support circuits 710 for programming and reading antifuses is shown in Figure 7B according to an embodiment of the present invention. The circuits 710 have many elements that are similar to the elements of the circuits 700 shown in Figure 7A, and elements common to
25 both of the circuits 700 and 710 have been given the same reference numerals and will not be described for purposes of brevity. The circuits 710 of Figure 7B include a bypass circuit 712 according to an embodiment of the present invention. The bypass circuit 712 shunts or bypasses current around the antifuse 516 in a manner similar to the bypass

circuit 702 of the circuits 700 shown in Figure 7A or the bypass circuit 270 of the antifuse bank 200 shown in Figure 2.

The bypass circuit 712 includes multiple p-channel transistors 714 coupled as diodes in series between the common bus line 520 and the well 523 of the antifuse 516.

5 Five diode-connected p-channel transistors 714 are shown in the bypass circuit 712, but more or less than the five diode-connected p-channel transistors 714 may be included in the bypass circuit 712 according to alternate embodiments of the present invention. The number of diode-connected p-channel transistors 714 in the bypass circuit 712 is determined with an analysis similar to the analysis described above to determine the
10 number of diodes 704 in the bypass circuit 702. A source of one of the transistors 714 is coupled to the common bus line 520, and a gate and a drain of another one of the transistors 714 is coupled to the well 523 of the antifuse 516. Others of the transistors 714 have a source coupled to a drain of a preceding transistor 714, and a gate and a drain coupled to a source of a succeeding transistor 714. The transistors 714 each have a
15 substrate coupled to the common bus line 520. The transistors 714 shunt or bypass a low level of current around the antifuse 516 from the common bus line 520 to the program driver circuit 510 during the programming mode when the elevated voltage is on the common bus line 520.

Several of the circuits in the antifuse bank 200 shown in Figure 2 are shown in
20 greater detail in Figure 7C. An electrical schematic diagram of several support circuits 720 for programming and reading antifuses is shown in Figure 7C according to an embodiment of the present invention. The circuits 720 have many elements that are similar to the elements of the circuits 700 shown in Figure 7A, and elements common to both of the circuits 700 and 720 have been given the same reference numerals and will
25 not be described for purposes of brevity.

The circuits 720 include the bypass circuit 702 shown and described with reference to Figure 7A that shunts or bypasses current around the antifuse 516. In addition, the gate bias circuit 508 is removed and replaced by a diode structure 722.

The gate terminal 530 of the HVT 524 is coupled to a cathode 724 of a diode 726, and an anode 728 of the diode 726 is coupled to Vcc. The diode 726 is forward biased as long as Vcc exceeds a voltage at the gate terminal 530. The gate terminal 530 is coupled to a cathode 730 of a diode 732. An anode 734 of the diode 732 is coupled to Vbb. The diodes 726 and 732 maintain the gate terminal 530 at a voltage slightly less than Vcc, or higher. The entire disclosure of U.S. Application Serial No. 09/652,429 entitled GATE DIELECTRIC ANTIFUSE CIRCUITS AND METHODS FOR OPERATING SAME and filed on August 31, 2000, is incorporated herein by reference, and includes figures and a description of a diode structure similar to the diode structure 722.

10 A voltage ramp rate on the common bus line 520 is low in alternate embodiments of the present invention to substantially prevent an excessive voltage across the antifuse 516 that may be caused by a limited current sourcing ability of the bypass circuits 702 or 712.

15 The program driver circuit 510 shown in Figures 5A, 5B, 5C, 7A, 7B, and 7C is different in alternate embodiments of the present invention. For example, different circuits 510 have different HVTs, or one may have a cascode coupling of the transistors 540 and 541 and the other may have only a single corresponding transistor 541. Different circuits 510 have different gate bias circuits or a diode structure such as those described with reference to Figures 5B, 5C, and 7C or different bypass circuits or pre-charge
20 circuits such as those described with reference to Figures 5B, 5C, 7A, 7B, and 7C according to alternate embodiments of the present invention.

 An electrical schematic diagram of support circuits 800 for programming and reading antifuses is shown in Figure 8 according to an embodiment of the present invention. The circuits 800 show in greater detail the adjustable resistors 572, 576, 582, and 586 and the HVTs 574 and 584 shown in Figure 5C. Each of the adjustable resistors
25 572, 576, 582, and 586 comprise resistors formed in parallel with fuses 802. The fuses 802 are short circuit connections that can be evaporated by a laser beam to create open circuits during the manufacture of an integrated circuit. One or more of the fuses 802 are

evaporated by the laser beam to set the impedance values of the adjustable resistors 572, 576, 582, and 586 to determine the voltage applied to the gate 530 of the HVT 524 and the pre-charge current supplied to the program driver circuit 510 through a node 820 during the programming mode of operation. The impedance values of the adjustable resistors 572, 576, 582, and 586 can also be set with a metal mask in a fabrication process that selects metal options to shunt the resistors according to alternate embodiments of the present invention.

An electrical schematic diagram of support circuits 900 for programming and reading antifuses is shown in Figure 9 according to an embodiment of the present invention. The circuits 900 show an alternative embodiment of the program driver circuit 510 and the read circuit 511 shown in Figure 5A. The circuits 900 also include the HVTs 590 and 592 shown in Figure 5C, the bypass circuit 712 shown in Figure 7B coupled in parallel with antifuses, and the node 820 shown in Figure 8. The bypass circuit 712 may also be called a diode stack.

An electrical schematic diagram of support circuits 1000 for programming and reading antifuses is shown in Figure 10 according to an embodiment of the present invention. The circuits 1000 show in greater detail HVTs that are shown in Figure 9.

In Figure 11 an electrical schematic diagram of the bypass circuit 712 is shown according to another embodiment of the present invention. The bypass circuit 712 includes multiple p-channel transistors coupled in series.

An electrical schematic diagram of support circuits 1200 for programming and reading antifuses is shown in Figure 12 according to an embodiment of the present invention. The circuits 1200 show the program driver circuit 510 and the read circuit 511 shown in Figure 5A in a block 1202 with additional circuits used to select and program antifuses.

The embodiments of the present invention shown and described herein help protect an unprogrammed antifuse from damage.

The antifuse 100 shown in Figure 1 and the transistors 300 and 400 shown in Figures 3 and 4 are formed in wells within other wells or tanks rather than the substrates shown in alternate embodiments of the present invention. Such wells or tanks may be situated with other wells or tanks, or within other wells or tanks, in a larger substrate.

5 The wells or tanks may also be situated in a silicon-on-insulator (SOI) device.

Circuits shown and described herein according to embodiments of the present invention, including the circuits shown in Figures 5A, 5B, 5C, 7A, 7B, and 7C include one or more HVTs. The same type of HVT is used several times in the same circuit, or combinations of the different HVTs 300 and 400 are used in the same circuit in alternate
10 embodiments of the present invention.

An integrated circuit fabricated with one or more of the antifuses and circuits described above may be tested in a test mode. For example, an integrated circuit having a bank of antifuses is prestressed by applying a prestress voltage that is less than the elevated voltage used to program the antifuses. The antifuses are exposed to the prestress
15 voltage and weaker antifuses are programmed as a result. The antifuses are then read to indicate the antifuses that have been programmed. The antifuses may be read by determining their analog resistances, by detecting a digital output of an addressed antifuse, or by detecting digital output from an addressed antifuse compared with several different load elements.

20 The entire disclosure of U.S. Application Serial No. 09/652,429 entitled GATE DIELECTRIC ANTIFUSE CIRCUITS AND METHODS FOR OPERATING SAME and filed on August 31, 2000, is incorporated herein by reference. The application Serial No. 09/652,429 discloses circuits such as read circuits and driver circuits that may be used with and coupled to the embodiments of the present invention described herein.

25 A block diagram of a static random access memory device (SRAM) 1300 is shown in Figure 13 according to an embodiment of the present invention. The SRAM 1300 may include one or more of the circuits and devices described above with respect to Figures 1-12 according to embodiments of the present invention. The SRAM 1300 has

an array 1310 of memory cells that are accessed according to address signals provided to the SRAM 1300 at a number of address inputs A0-A16. An address decoder 1320 decodes the address signals and accesses memory cells in the array 1310 according to the address signals. Data is written to the memory cells in the array 1310 when a write enable signal WE* and a chip enable signal CE* coupled to the SRAM 1300 are both low. The data is received by the SRAM 1300 over eight data input/output (I/O) paths DQ1-DQ8. The data is coupled to the memory cells in the array 1310 from the I/O paths DQ1-DQ8 through an I/O control circuit 1330. Data is read from the memory cells in the array 1310 when the write enable signal WE* is high and an output enable signal OE* coupled to the SRAM 1300 and the chip enable signal CE* are both low. A power down circuit 1340 controls the SRAM 1300 during a power-down mode. The circuits and devices described above with respect to Figures 1-12 according to embodiments of the present invention may be included in other types of memory devices such as DRAMs, programmable logic devices, PROMs, EPROMs, and EEPROMs.

An integrated circuit package 1400 of a 32k x 36 SRAM memory device is shown in Figure 14 according to an embodiment of the present invention. The SRAM includes one or more of the circuits and devices described above with respect to Figures 1-13 according to embodiments of the present invention. One of the external pins 220 or 522 described above is one of several pins 16, 38, 39, 42, 43, or 66 in the package 1400. The pins 16, 38, 39, 42, 43, or 66 are non-reserved pins, one of which is used as one of the external pins 220 or 522. The pin selected as one of the external pins 220 or 522 will be coupled to an elevated voltage if an antifuse in the SRAM is to be programmed. The selected pin may be left floating, or may be coupled to the read voltage VREAD during a normal operation of the SRAM.

A block diagram of an information-handling system 1500 is shown in Figure 15 according to an embodiment of the present invention. The information-handling system 1500 includes a memory system 1508, a processor 1510, a display unit 1520, and an input/output (I/O) subsystem 1530. The processor 1510 may be, for example, a

microprocessor. One or more of the memory system 1508, the processor 1510, the display unit 1520, and the I/O subsystem 1530 may include one or more of the circuits and devices described above with respect to Figures 1-14 according to embodiments of the present invention. The processor 1510, the display unit 1520, the I/O subsystem
5 1530, and the memory system 1508 are coupled together by a suitable communication line or bus 1540 over which signals are exchanged between them.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those skilled in the art having the benefit of this description that any equivalent arrangement may be substituted for the specific embodiments shown. For
10 example, specific memory devices have been described and shown in the Figures. One skilled in the art having the benefit of this description will recognize that the embodiments of the present invention may be employed in other types of memory devices and in other types of integrated circuit devices. The voltage V_{bb} described above may be approximately equal to V_{ss} , or may be negative. In addition, in alternate embodiments of
15 the present invention, the common bus line is sized to provide a programming current for more than one antifuse at the same time. The present invention is therefore limited only by the claims and equivalents thereof.